

## CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
  - 2 an internal test bus (ITB);
  - 3 a plurality of deskew clusters coupled to the ITB,
  - 4 wherein the plurality of deskew clusters each include a
  - 5 deskew controller;
  - 6 an integrated test controller (ITC) coupled to the ITB;
  - 7 and
  - 8 a debug unit coupled to the ITC;
  - 9 wherein the ITC generates a single global control signal and
  - 10 the deskew controller generates a first local command signal.
- 1 2. The apparatus of claim 1, wherein the plurality of
  - 2 deskew clusters further comprise a plurality of deskew
  - 3 buffers and a regional clock driver (RCD).
- 1 3. The apparatus of claim 1, further comprising a second
  - 2 local command signal, wherein the single global control
  - 3 signal and one of the first local command signal, the second
  - 4 local command signal, and both the first local command signal
  - 5 and the second local command signal provide a distributed
  - 6 test control scheme for integrated circuits including debug
  - 7 and testability operations.
- 1 4. The apparatus of claim 1, wherein the first local
  - 2 command signal is a snapshot instruction and the second local

3 command signal is a shift instruction.

1 5. The apparatus of claim 4, wherein a snapshot instruction  
2 can be issued at a first time period and a shift instruction  
3 can be issued at a second time period, and results from the  
4 snapshot instruction can be shifted by the shift instruction  
5 after a third period of time.

1 6. A method comprising:

2 generating a single global control signal in an  
3 integrated test controller;

4 decoding the single global control signal in a deskew  
5 controller;

6 generating a first local command signal corresponding to  
7 the single global control signal;

8 distributing the first local command signal to a  
9 regional clock driver (RCD); and

10 performing one of a debug operation and a testability  
11 operation on an integrated circuit by using the single global  
12 control signal and the first local command signal.

1 7. The method of claim 6, further comprising generating a  
2 second local command signal corresponding to the single  
3 global control signal.

1 8. The method of claim 7, wherein one of the first local  
2 command signal is a snapshot instruction and the second local  
3 command signal is a shift instruction.

- 1 9. The method of claim 8, further comprising issuing a  
2 snapshot instruction at a first time period;  
3 issuing a shift instruction at a second time period; and  
4 shifting results from the snapshot instruction by the shift  
5 instruction after a third period of time.
- 1 10. The method of claim 6, further comprising triggering the  
2 debug operation after a variable time period.
- 1 11. A program storage device readable by a machine  
2 comprising instructions that cause the machine to:  
3 generate a single global control signal in an integrated  
4 test controller;  
5 decode the single global control signal in a deskew  
6 controller;  
7 generate a first local command signal corresponding to  
8 the single global control signal;  
9 distribute the first local command signal to a regional  
10 clock driver (RCD); and  
11 perform one of a debug operation and a testability  
12 operation on an integrated circuit by using the single global  
13 control signal and the first local command signal.
- 1 12. The program storage device of claim 11, wherein the  
2 instructions further cause the machine to:  
3 generate a second local command signal corresponding to

4 the single global control signal.

1 13. The program storage device of claim 12, wherein the  
2 first local command signal is a snapshot operation and the  
3 second local command signal is a shift operation.

1 14. The program storage device of claim 13, wherein the  
2 instructions further cause the machine to: issue a snapshot  
3 operation at a first time period;

4 issue a shift operation at a second time period; and shift  
5 results from the snapshot operation by the shift operation  
6 after a third period of time.

1 15. The program storage device of claim 11, the instructions  
2 further cause the machine to: trigger the debug operation  
3 after a variable time period.